WHAT IS CLAIMED IS:

1. A nonvolatile memory apparatus comprising a nonvolatile memory and a controller,

wherein said nonvolatile memory has a plurality of nonvolatile memory cells each capable of storing information of n bits (n: integer of 2 or larger), and can perform a first reading operation of outputting information read from said nonvolatile memory cell as information of m bits (m: integer smaller than n) and a second reading operation of outputting information read from said nonvolatile memory cell as information of n bits, and

wherein said controller performs the first reading operation to read first information from said nonvolatile memory and performs the second reading operation to read second information from said nonvolatile memory.

2. The nonvolatile memory apparatus according to claim 1, wherein said first information is validity management information indicative of validity of a storage area of said second information.

3. The nonvolatile memory apparatus according to claim 2, wherein when the nonvolatile memory is operated according to an instruction from the controller, said controller checks validity of a storage area of said second information on the basis of the validity

management information read from the nonvolatile memory by performing the first reading operation and, when it is determined that the storage area is valid, performs the second reading operation to read the second information from the nonvolatile memory.

4. The nonvolatile memory apparatus according to claim 3, wherein said controller checks validity of a storage area of said second information on the basis of validity management information read from the nonvolatile memory by performing the first reading operation, when it is determined that the storage area is invalid, checks validity of the storage area of said second information on the basis of the validity management information read from the nonvolatile memory by performing the first reading operation on an alternative area of the storage area of said second information and, when the storage area is valid, performs the second reading operation to read the second information from the alternative area.

5. The nonvolatile memory apparatus according to claim 1,

wherein said nonvolatile memory cell has a threshold voltage included in one of four or more threshold voltage distributions according to information to be stored, and

wherein at the time of storing said first information into said nonvolatile memory cell, said nonvolatile memory uses a predetermined voltage between said threshold voltage distributions as a boundary, sets, as the threshold voltage of the nonvolatile memory, any of threshold voltage distributions of voltages higher than said predetermined voltage or threshold voltage distributions of voltages lower than said predetermined voltage, and compares said predetermined voltage with the threshold voltage of a nonvolatile memory cell in said first reading operation, thereby reading m-bit information.

6. The nonvolatile memory apparatus according to claim 5, wherein the threshold voltage of a nonvolatile memory cell in which said first information is stored is a voltage selected from a voltage in an upper-limit threshold voltage distribution and a voltage in a lower-limit threshold voltage distribution.

7. The nonvolatile memory apparatus according to claim 1,

wherein said controller can output second information read from the nonvolatile memory by said second reading operation to the outside, and can supply said second information input from the outside to the nonvolatile memory, and

wherein said nonvolatile memory has a memory buffer which can temporarily store second information read by said second reading operation before the second information is supplied to said controller and can temporarily store second information supplied from said controller before said second information is stored into said nonvolatile memory cell.

8. The nonvolatile memory apparatus according to claim 7, wherein said nonvolatile memory outputs first information by bypassing said memory buffer at the time of reading first information by said first reading operation.

9. The nonvolatile memory apparatus according to claim 8, wherein said first information includes validity management information indicative of validity of a storage area of said second information.

10. The nonvolatile memory apparatus according to claim 9, wherein when the nonvolatile memory is operated according to an instruction from the controller, said controller checks validity of a storage area of said second information on the basis of validity management information read from the nonvolatile memory by performing the first reading operation and, when it is determined that the storage area is valid, writes the

second information of said memory buffer into a memory cell.

11. The nonvolatile memory apparatus according to claim 10, wherein said controller checks validity of a storage area of said second information on the basis of validity management information read from the nonvolatile memory by performing the first reading operation, when it is determined that the storage area is invalid, checks validity of the storage area of said second information on the basis of validity management information read from the nonvolatile memory by performing the first reading operation on an alternative area of the storage area of said second information and, when the storage area is valid, writes the second information in the memory buffer into a memory cell in the alternative area.

12. The nonvolatile memory apparatus according to claim 7, wherein said controller has a controller buffer for temporarily holding second information supplied from the outside and temporarily holding second information read from the nonvolatile memory and supplied.

13. The nonvolatile memory apparatus according to claim 12, wherein said controller supplies data from the controller buffer to the memory buffer, after that,

stores the data in the memory buffer to a nonvolatile memory cell and, in parallel with the storing operation, can input another data from the outside into the controller buffer.

14. A nonvolatile memory apparatus comprising a nonvolatile memory and a controller,

wherein said nonvolatile memory has a plurality of nonvolatile memory cells each of which can be set in an information storing state included in one of four or more information storing states, and can perform a first reading operation of outputting information read from said nonvolatile memory cell which is set in said information storing state as information of m bits (m: integer of 1 or larger) and a second reading operation of outputting information read from said nonvolatile memory cell which is set in said information storing state as information of n bits (n: integer larger than m), and

wherein said controller performs the first reading operation to read first information from said nonvolatile memory and performs the second reading operation to read second information from said nonvolatile memory.

15. The nonvolatile memory apparatus according to claim 14, wherein an information storing state included in one of said four or more information storing states is a threshold voltage state included in one of four or

more threshold voltage distributions of a nonvolatile memory cell.

16. The nonvolatile memory apparatus according to claim 15, wherein at the time of storing said first information into said nonvolatile memory cell, said nonvolatile memory sets, as a threshold voltage of the nonvolatile memory cell, a voltage selected from a voltage in said threshold voltage distribution of the upper limit and a voltage in said threshold voltage distribution of the lower limit.

17. The nonvolatile memory apparatus according to claim 16,

wherein said nonvolatile memory has a memory buffer which can hold second information read as n-bit information from each of a plurality of nonvolatile memory cells by said second reading operation, supply the second information to the controller, hold second information supplied from said controller, and set one nonvolatile memory cell every n bits, at a threshold voltage included in one of four threshold voltage distributions, and

wherein the first information read as m-bit information from each of the plurality of nonvolatile memory cells by said first reading operation is output to said controller while bypassing said memory buffer.